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DIGITAL COMMUNICATIONS LABORATORY

KURUKSHETRA UNIVERSITY , KURUKSHETRA

DEPARTMENTOF
ELECTRONICS & COMMUNICATION ENGINEERING
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RN COLLEGE OF ENGINEERING & TECHNOLOGY
Department of ECE

DIGITAL COMMUNICATIONS LAB FILE

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Electronics and Communication Engineering

List of Experiments in Digital Communication Lab:

1) To design and study the working of ASK modulation and demodulation system with the help of suitable circuit.
2) To generate the Pulse Amplitude modulated signal and demodulated signals.
3) To generate the pulse width modulated and demodulated signals
4) To generate pulse position modulation and demodulation signals and to study the effect of amplitude of the modulating signal on output
5) To study and verify the sampling theorem and reconstruction of sampled wave form.
6) To study the Delta modulation process by comparing the present signal with the
7) To study frequency shift key (FSK) Modulator and Demodulator
8) To study the characteristics of the PSK Modulation & Demodulation techniques
9) To study the various steps involved in generating differential phase shift keyed signal at the modulator end and recovering the binary

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1. Amplitude Shift Keying- Modulation & Demodulation

Aim: To design and study the working of ASK modulation and demodulation system with the help of suitable circuit.

Apparatus required:

1. 2 Signal generators,
2. Resisters 39K- 2, 3.3K -2, SL 100 transistor-1
3. CRO
4. BNC probes, connecting wires.

Theory:

The transmission of digital signals is increasing at a rapid rate. Low-frequency analog signals are often converted to digital format (PAM) before transmission.

The source signals are generally referred to as baseband signals. We can send analog and digital signals directly over a medium. From electro-magnetic theory, for efficient radiation of electrical energy from an antenna it must be at least in the order of magnitude of a wavelength in size; $c = f\lambda$, where c is the velocity of light, f is the signal frequency and λ is the wavelength. For a 1kHz audio signal, the wavelength is 300 km. An antenna of this size is not practical for efficient transmission. The low-frequency signal is often frequency-translated to a higher frequency range for efficient transmission. The process is called modulation. The use of a higher frequency range reduces antenna size.

ASK:

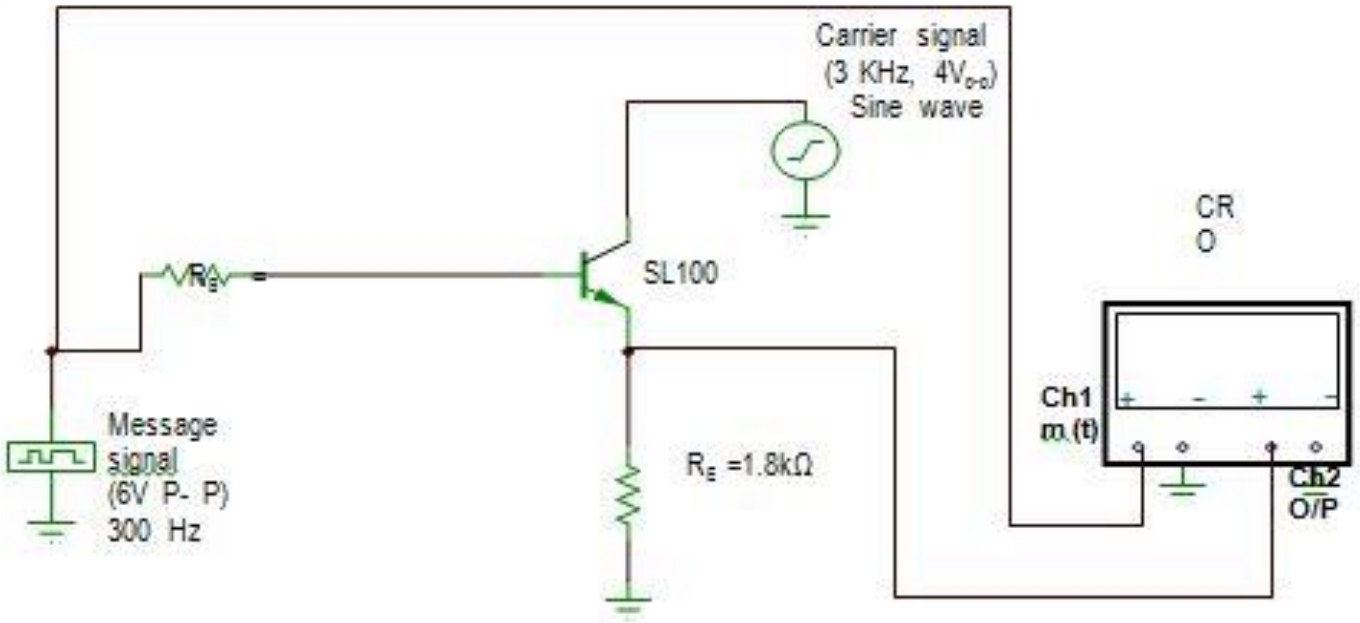
Amplitude shift keying - ASK - in the context of digital communications is a modulation process, which imparts to a sinusoid two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message.

For a binary message sequence there are two levels, one of which is typically zero. Thus the modulated waveform consists of bursts of a sinusoid.

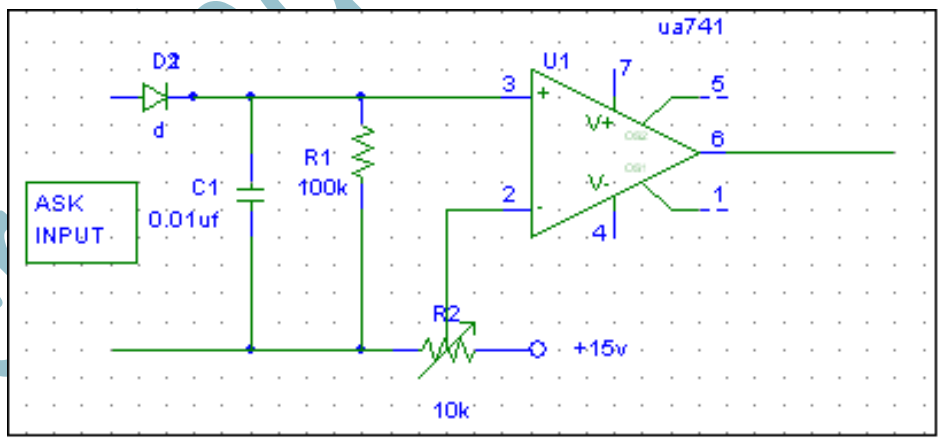
A binary ASK (BASK) wave is obtained by multiplying the message signal with the carrier. The B-ASK signal has two levels „1" and „0" representing the presence and absence of the sinusoid respectively. This can be shown in the waveform below. The message signal must be represented in NZR uni polar format only. Binary ASK system has the largest probability of bit error when compared to FSK and PSK systems.
There are sharp discontinuities shown at the transition points. These result in the signal having an unnecessarily wide bandwidth. Band limiting is generally introduced before transmission, in which case these discontinuities would be „rounded off". The band limiting may be applied to the digital message, or the modulated signal itself.

One of the disadvantages of ASK, compared with FSK and PSK, for example, is that it has not got a constant envelope. This makes its processing (eg, power amplification) more difficult, since linearity becomes an important factor. However, it does make for ease of demodulation with an envelope

Circuit Diagram: (Modulation)



Circuit Diagram: (De-Modulation)



DESIGN:

V_{BE} = 0.7 V, V_{CE} (Sat) =0.3V
I_C=1mA, β=50, I_E = I_C

Applying KVL to O/P

V_C Peak $-V_{CE}-I_ER_E=0 \Rightarrow 2-0.3-(1\times10^{-3})R_E=0$

R_E=1.7KΩ ≈ 1.8KΩ

Applying KVL to O/P, $V_{m(peak)} = 3V$

$V_m(Peak) - I_BR_B - V_{BE} - I_ER_E=0$, Where $I_ER_E = (1\times10^{-3}\times1.8k\Omega)$

$3 - 1X10^{-3} R_B - 0.7 - 1.7 = 0$

R_B =30 KΩ≈ 39 KΩ

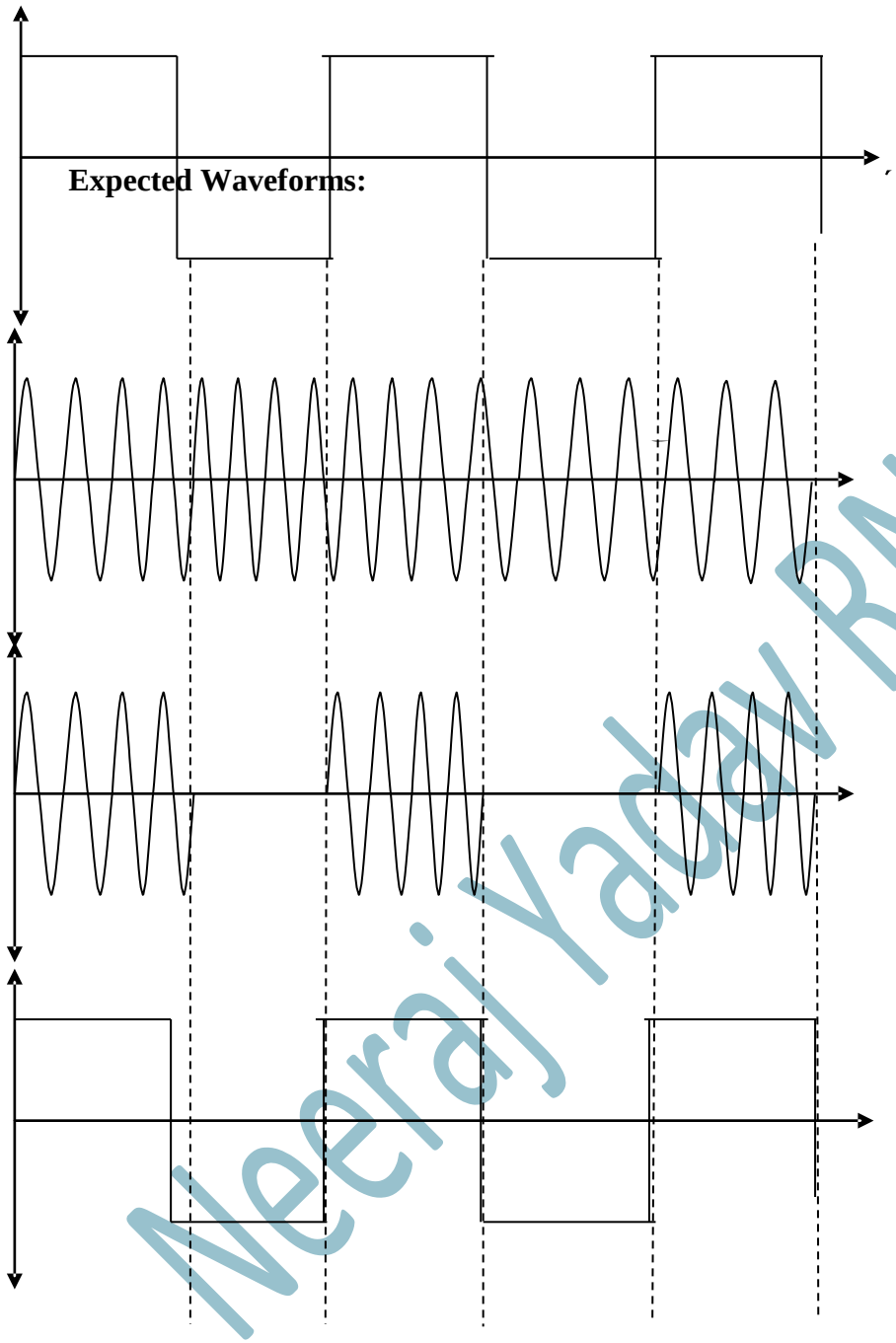
Design Demodulation

$1/Wc < R_1C_1 < 1/W$, Let c = 0.01μf ; R_1C_1 = 1ms; R_1 = 100kΩ

PROCEDURE:

1) The circuit connections are made as per the circuit diagram.
2) A message signal with frequency about 150 Hz and amplitude of about 5 volts is fed to the transistor and carrier is fed to the collector (nearly 5 volts).
3) ASK output is now drawn at the collector.
4) This ASK output is fed to the demodulator circuit and the message signal at the output is obtained.
5) The modulated and the modulating signal are drawn on a graph.

Expected Waveforms:



Result : ASK Modulation & Demodulation successfully studied.

2. Pulse Amplitude and Modulation

Aim: To generate the Pulse Amplitude modulated signal and demodulated signals.

Apparatus required:

1.Pulse amplitude modulation trainer.

2. Signal generator

3. CRO

4. BNC probes, connecting wires.

Theory:

PAM is the simplest form of the data modulation. The amplitude of uniformly spaced pulses is varied in proportion to the corresponding sample values of a continuous message m(t).

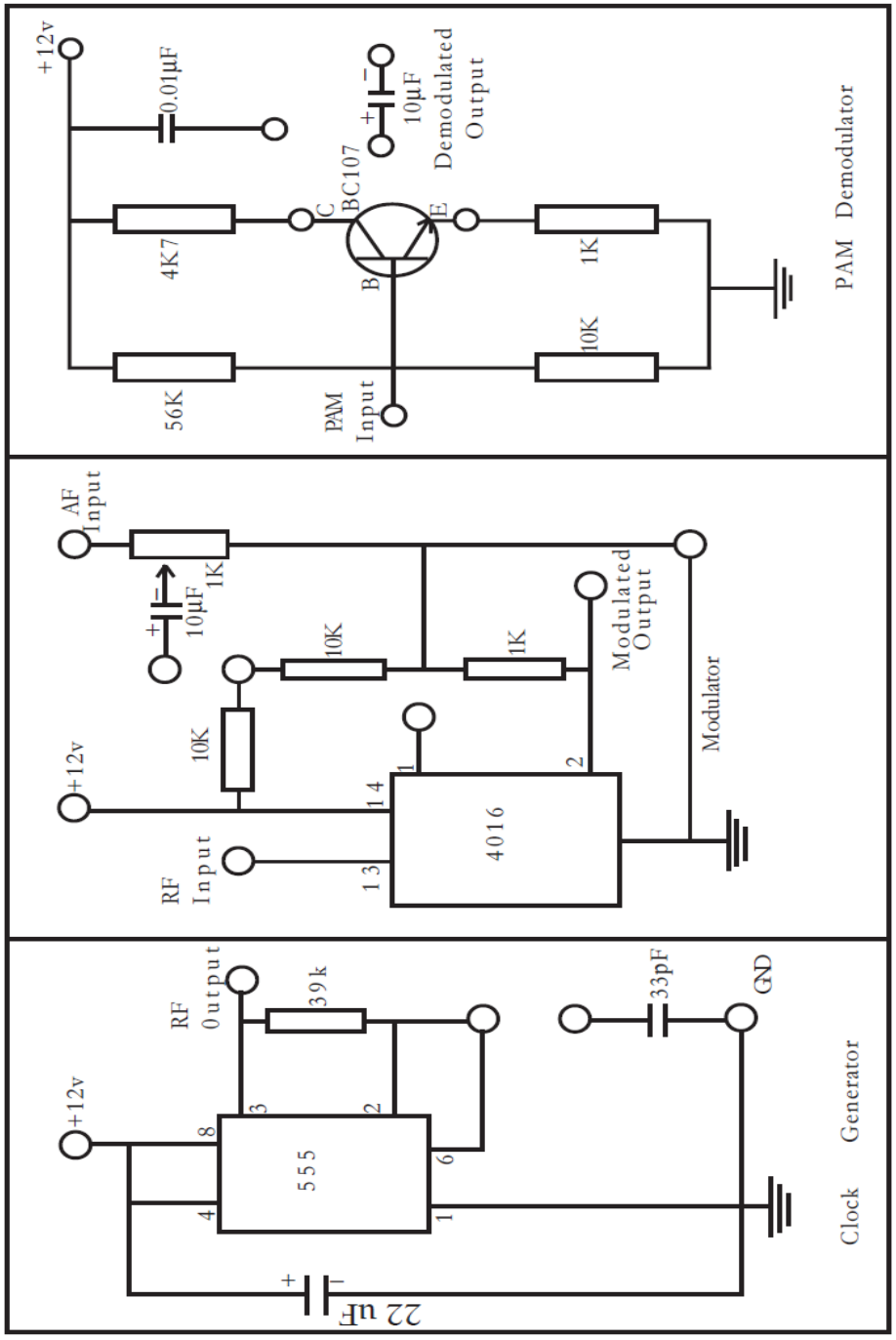
A PAM waveform consists of a sequence of list-topped pulses. The amplitude of each pulse corresponds to the value of the message signal x(t) at the leading edge of the pulse.

The pulse amplitude modulation is the process in which the amplitude of regularity spaced rectangular pulses vary with the instantaneous sample values of a continuous message signal in a one-one fashion.

PAM is of two types :

1. Double polarity PAM – This is the PAM wave which consists of both positive and negative pulses.
2. Single polarity PAM – This consists of PAM wave of only either negative or positive pulses. In this the fixed dc level added to the signal to ensure single polarity signal.

Circuit Diagram:



CONNECTION CIRCUIT DIAGRAM OF PAM

Procedure:

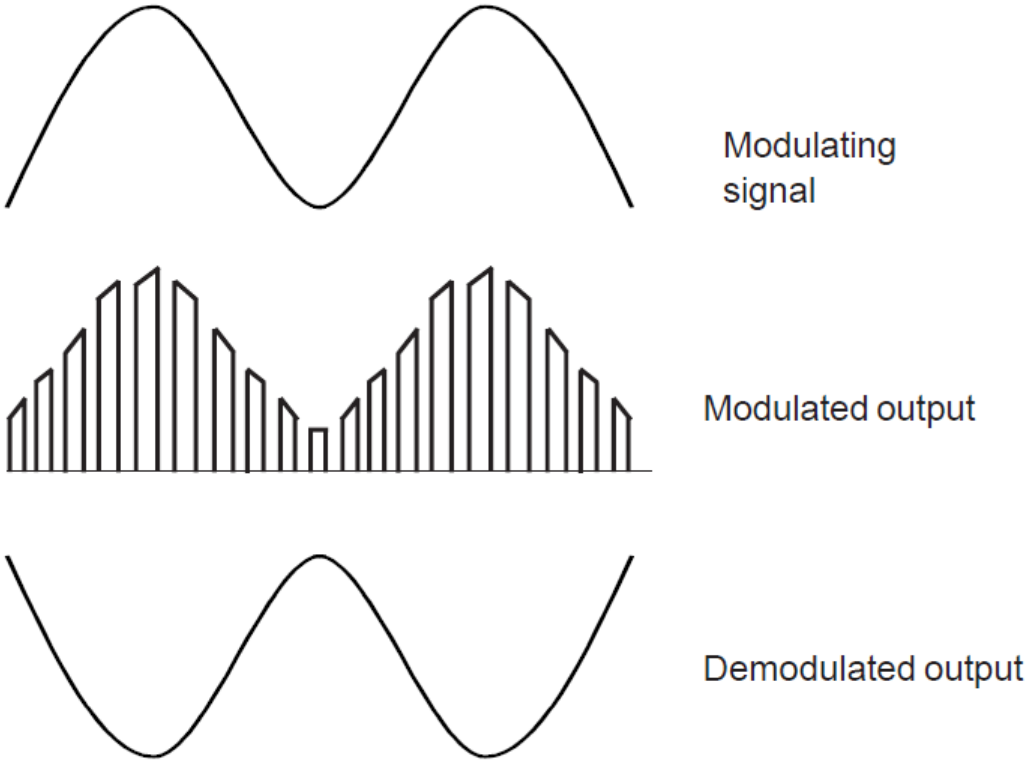
1. Switch on pulse Amplitude modulation and demodulation trainer.
2. In clock generator section connect pin 6 of 555IC to the 33pfcapacitor terminal.
3. Check the clock generator (RF)output signal.
4. Connect RF output of clock generator to the RF input of modulator section.
5. Connect a 1KHz; 2vp-p of sine wave from function generator to the AF input of modulator section.
6. Short the 10F terminal and 10k terminal of modulator.
7. Connect 10k terminal to pin 1 of IC 4016.
8. Connect the CRO to modulated output of modulator section.
9. Adjust the 1k potentiometer to vary the amplitude of the modulated signal.
10. Adjust the AF signal frequency from 1KHZ-10KHZ to get stable output waveform. While increases the AF signal frequency decreases the output signal pulses.
11. During demodulation, connect the modulated output to the PAM input of Demodulator section.
12. Connect channel 1 of CRO to modulating signal and channel-2 to demodulated output. Observe the two waveforms that they are 1800out of phase, since the transistor detector operates in CE configuration.

Sample Readings:

RF frequency = 1KHz RF Voltage = 5 Volt

S. No	AF input voltage V_{p-p} (volts)	RF Voltage V_{p-p} (volts)	PAM output voltage	
			V_{max} (volts)	V_{min} (volts)

Expected Waveforms:



Result: Study of PAM Modulation & Demodulation is completed successfully.

3. PULSE WIDTH MODULATION AND DEMODULATION

Aim: To generate the pulse width modulated and demodulated signals

Apparatus required:

1. Pulse width modulation and Demodulation Trainer.
2. CRO
3. BNC probes and Connecting Wires

Theory:

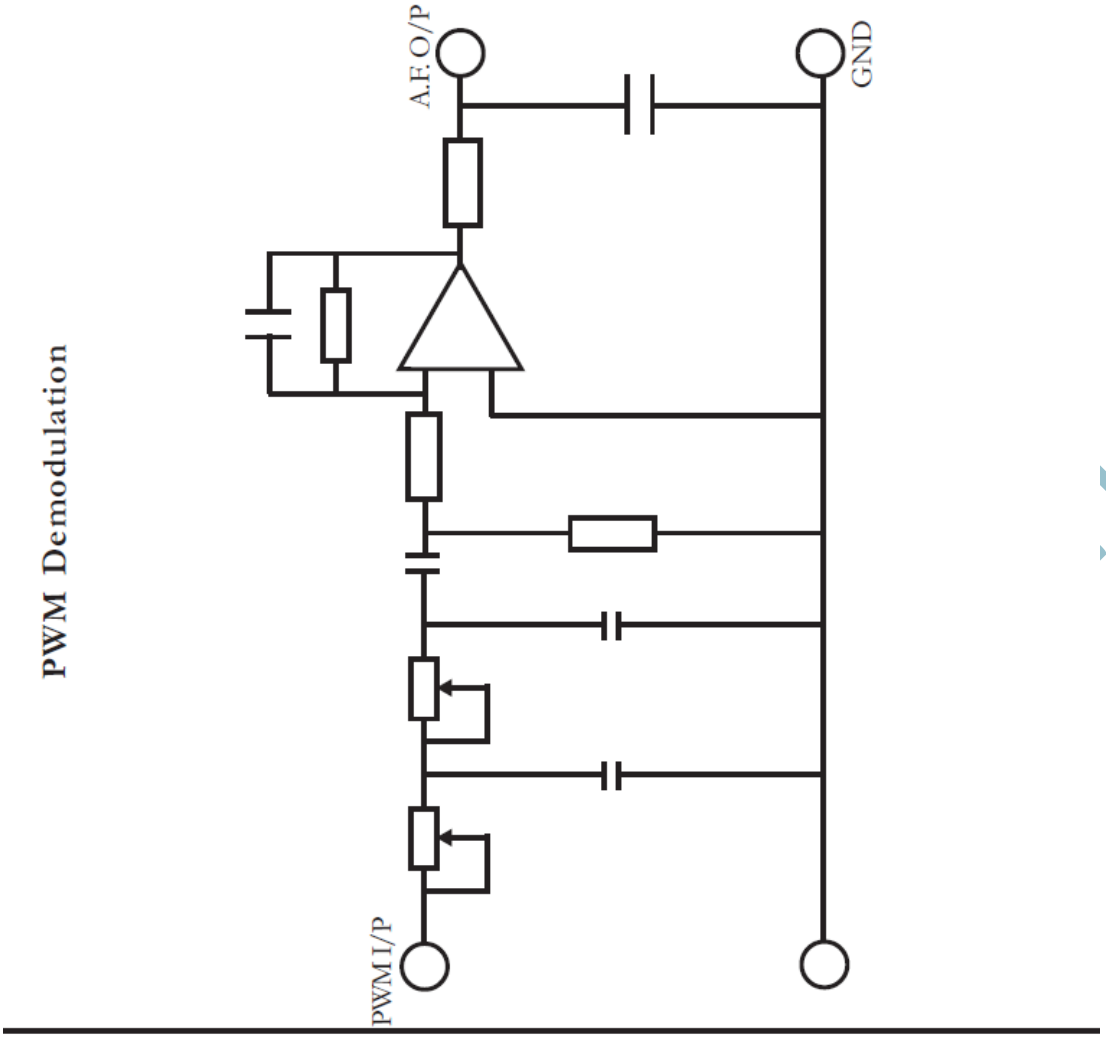
In PWM, the samples of the message signal are used to vary the duration of the individual pulses. Width may be varied by varying the time of occurrence of leading edge, the trailing edge or both the edges of the pulse in accordance with modulating wave. It is also called Pulse Duration Modulation.

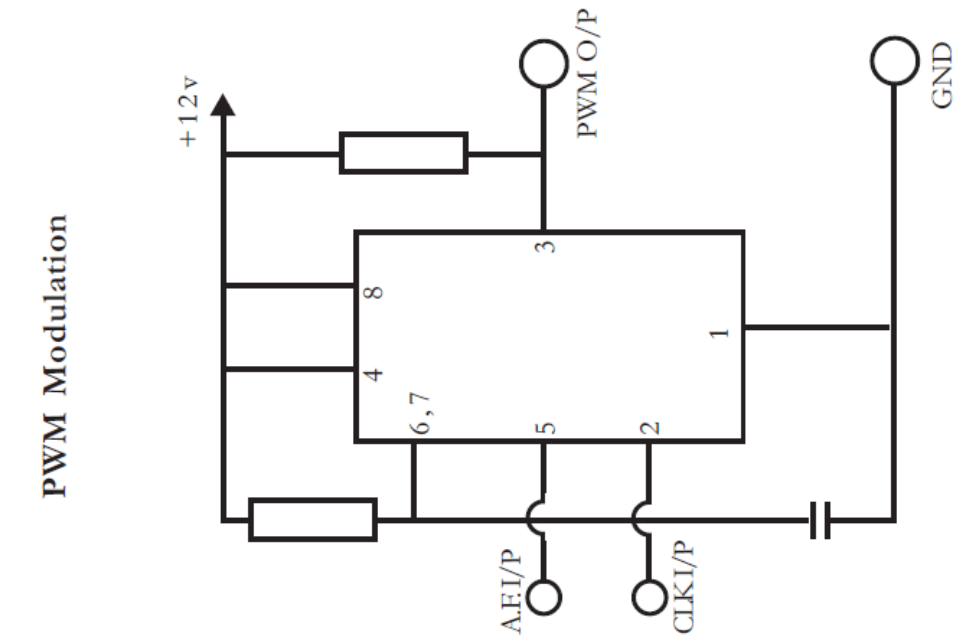
Procedure:

1) Switch on Pulse width modulation and Demodulation trainer .
2) Connect the Clock O/P to the clock I/P terminal of PWM modulation.
3) Connect the AF O/P to AF I/P terminal of PWM modulation.
4) Observe the PWM O/P at pin 3 of 555 IC on CRO.
5) By varying frequency and amplitude of the modulating signal, observe the corresponding change in the width of the output pulses.
6) During demodulation, connect the PWM O/P of PWM modulation to the PWM I/P of PWM demodulation.
7) Observe the demodulated output at AF O/P of PWM demodulation on CRO.

Observations:

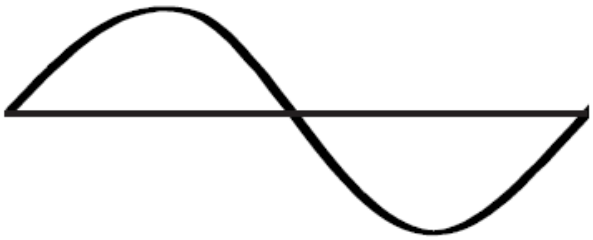
S.No	Control Voltage(V)	o/p pulse width (msec)


PWM Demodulation
A.F. O/P
GND
PWM I/P


PWM Modulation
+12v
PWM O/P
GND
3
8
4
6, 7
5
2
1
A.E I/P
CLK I/P

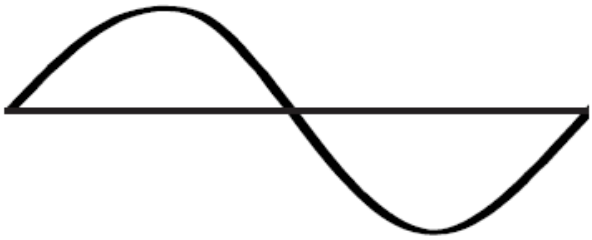
Expected Wave forms:

Clock Pulse



A.F.Signal

PWM O/P



Demodulated Signal

Result: PWM Signals Modulated & Demodulated successfully.

Aim: To generate pulse position modulation and demodulation signals and to study the effect of amplitude of the modulating signal on output.

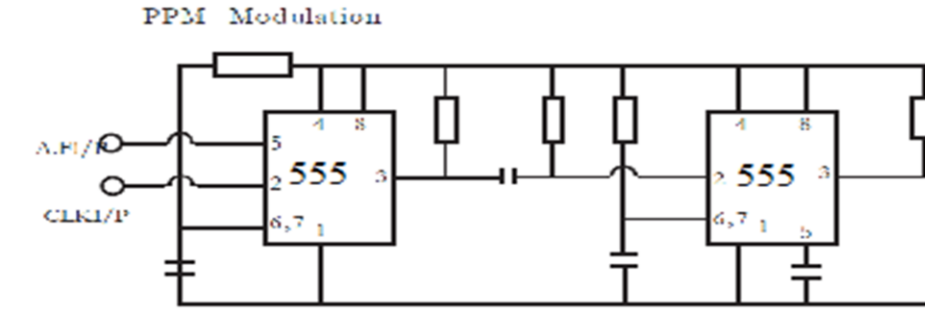
Apparatus required:

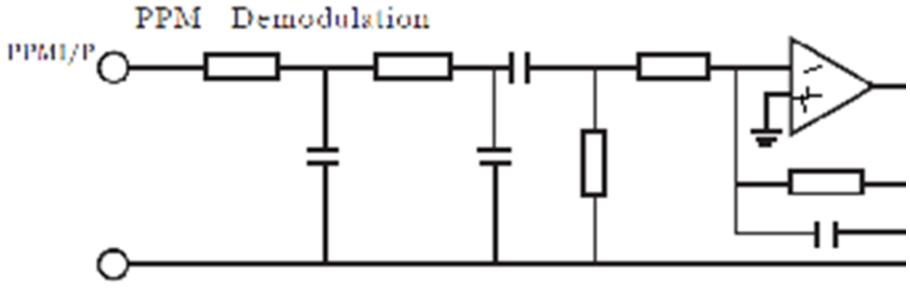
1. Pulse position modulation and demodulation trainer.
2. CRO
3. BNC probes and Connecting Wires

Theory:

In Pulse Position Modulation, both the pulse amplitude and pulse duration are held constant but the position of the pulse is varied in proportional to the sampled values of the message signal. Pulse time modulation is a class of signaling technique that encodes the sample values of an analog signal on to the time axis of a digital signal and it is analogous to angle modulation techniques. The two main types PTM are PWM and PPM. In PPM the analog sample value determines the position of a narrow pulse relative to the clocking time. In PPM rise time of pulse decides the channel bandwidth. It has low noise interference.

Circuit Diagram:



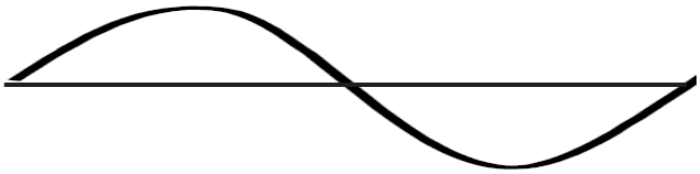


Procedure:

1. Switch on PPM modulator and demodulator trainer.
2 . Connect the Clk O/P to the Pin 2 of 555 IC.
3 . Connect the AF O/P to the pin 5 of 555 IC.
4 . Observe the PPM O/P at pin 3 of second IC 555 on CRO.
5 . Connect the PPM O/P to the PPM I/P of PPM demodulation.
6. Observe the demodulated O/P on CRO**.**

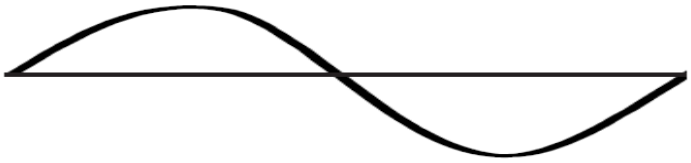
Expected Waveforms:

Clock Signal



A.F.Signal

PPM O/P



Demodulated O/P

Result: Modulation & Demodulation of PPM is done successfully.

5. Sampling Theorem – Verification

Aim: To study and verify the sampling theorem and reconstruction of sampled wave form.

Apparatus Required:

1. PHYSITECH's Sampling Theorem Trainer Kit
2. Function Generator
3. CRO
4. Connecting wires.
5. BNC Probes.

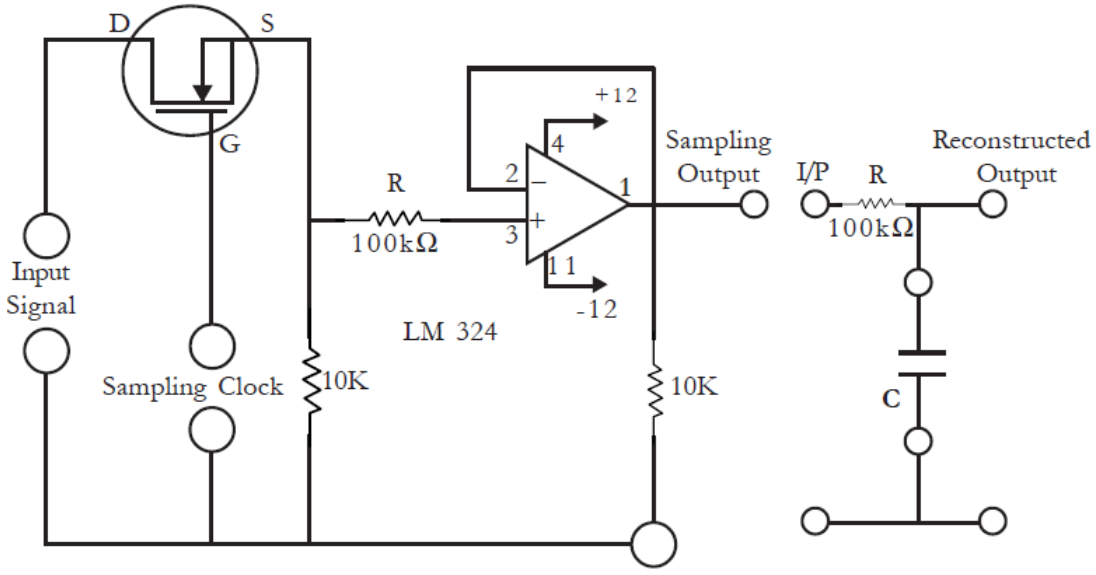
Theory:

The analog signal can be converted into a discrete time signal by a process called sampling. The sampling theorem for a band limited signal of a finite energy can be stated as

"A band limited signal of finite energy which has no frequency component higher than W Hz is completely described by specifying the values of the signal at instants of time separated by 1/2W seconds".

It can be recovered from the knowledge of the samples taken at the rate of 2W per second.

Circuit Diagram:



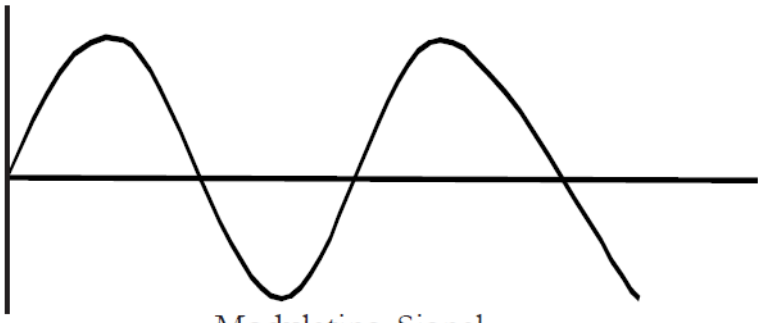
Circuit Diagram for Verfication of Sampling Theorem

Procedure:

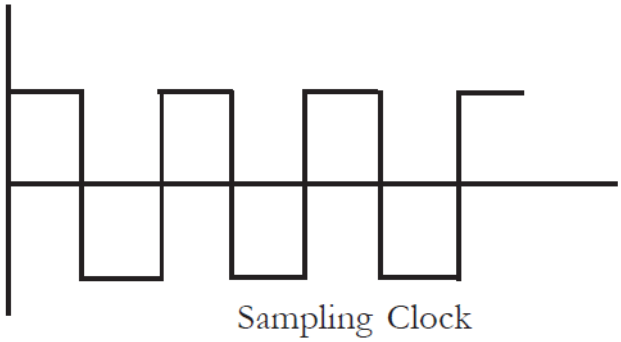
1. Connections are made as per the Circuit diagram.
2. Apply the input signal with a frequency of 500Hz (VP-P) using a function generator.
3. Sampling clock frequency which is variable of 3KHz to 50KHz should be connected across the terminals which is indicated.
4. Now observe the sampling output of the circuit at the o/p.
5. By using the capacitors provided on the trainer, reconstruct the signal and verify it with the given input.
6. Reconstructed signal voltage will be depends on capacitor value.
7. Vary the sampling frequency and study the change in reconstructed signal.
8. If the sampling clock frequency is below 20KHz you will observe the distorted demodulated output**.**

Observations:

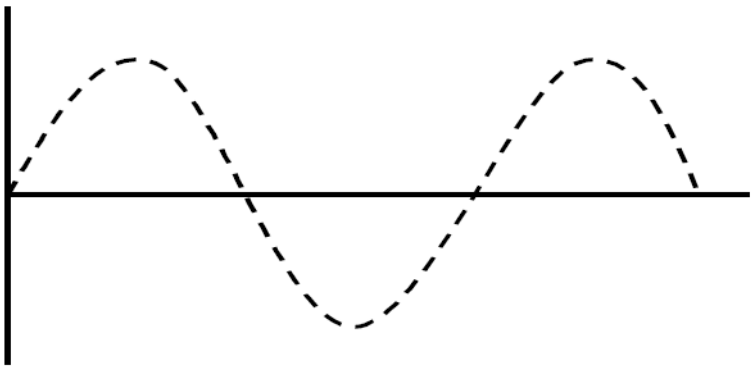
S. No	Cases	Message signal frequency (f_m KHz)	Smpling frequency (f_s KHz)	Inference



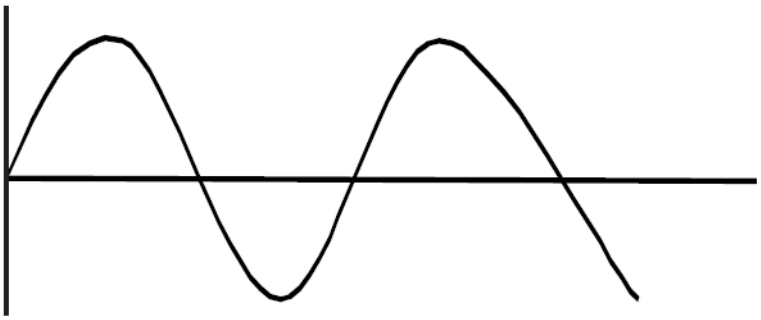
Modulating Signal



Sampling Clock



Sampling Output



Demodulating Signal

Result: Sampling theorem and reconstruction of sampled wave form has been successfully

studied

6 DELTA MODULATION & DEMODULATION

Aim: To study the Delta modulation process by comparing the present signal with the previous signal of the given modulating signal.

APPARATUS:

1. Delta Modulation trainer
2. CRO
3. Connecting wires.

Theory:

DM uses a single bit PCM code to achieve to achieve digital transmission of analog signal. With conventional PCM each code is binary representation of both sign and magnitude of a particular sample. With DM, rather than transmitting a coded representation of a sample a single bit is transmitted, which indicates whether the sample

is smaller or larger than the previous sample. The algorithm for a delta modulation system

is a simple one. If the current sample is smaller than the previous sample then logic 0 is transmitted or logic 1 is transmitted if the current sample is larger than the previous sample. The input analog is sampled and converted to a PAM signal followed by comparing it with the output of the DAC. The output of the DAC is equal to the regenerated magnitude of the previous sample which was stored in the up/down counter

as a binary number. The up/down counter is incremented or decremented whether the previous sample is larger or smaller than the current sample. The up/down counter is clocked at a rate equal to the sample rate. So, the up/down counter is updated after each comparison.

Procedure:

1. Switch on the experimental board
2. Connect the clock signal of Bit clock generator to the bit clock input of Delta modulator circuit.

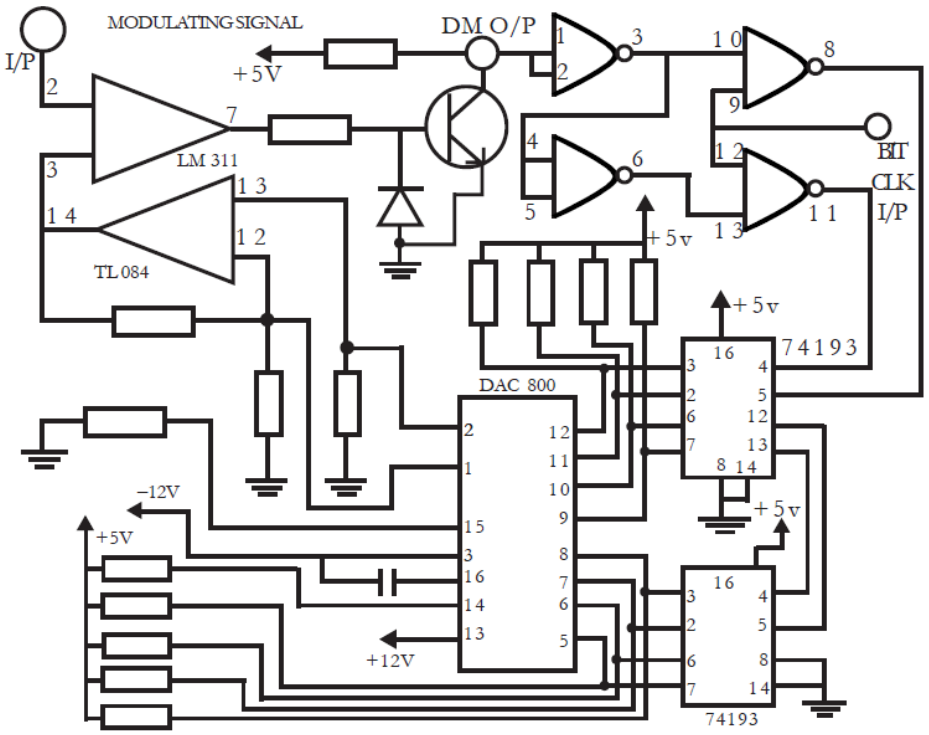
3. Connect modulating signal of the modulating signal generator to the modulating signal input of the Delta modulator.
4. Observe the modulating signal on Channel 1 of CRO
5. Observe the Delta modulator output on channel 2 of CRO
6. Connect the DM o/p of modulator to the DM I/P of Demodulator circuit.

7. Connect the clock signal to the Bit clock I/P of Demodulator circuit.
8. Observe the demodulated o/p on channel 2 of CRO.
9. Connect the demodulated o/p to the filter input of demodulator circuit.
10. Observe the demodulated o/p with filter on CRO.

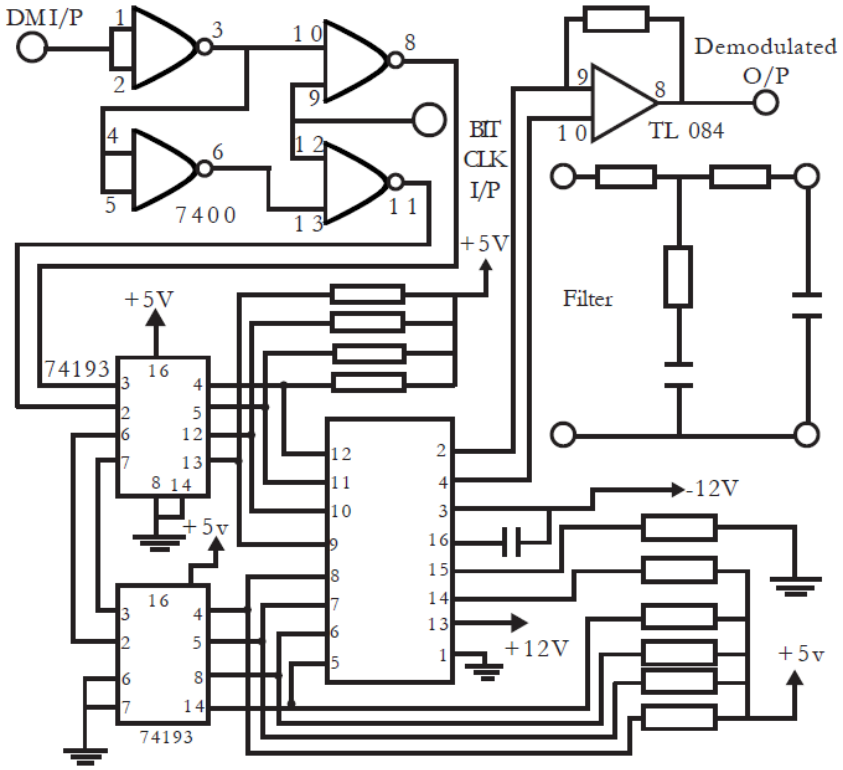
Delta Modulation & Demodulation

Circuit Diagram :

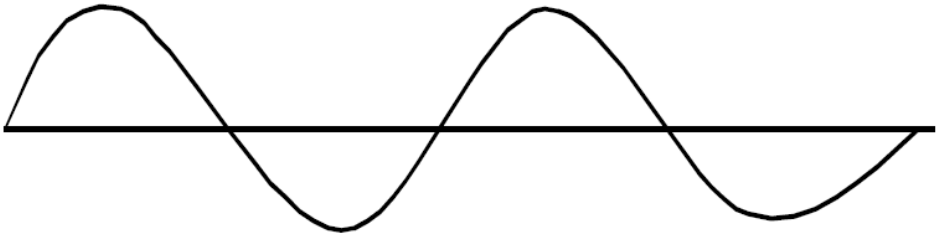
Modulator



Demodulator

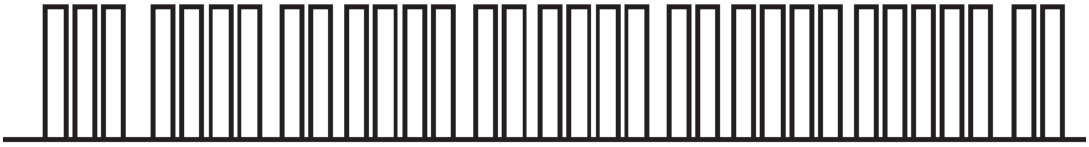


Expected Waveforms:

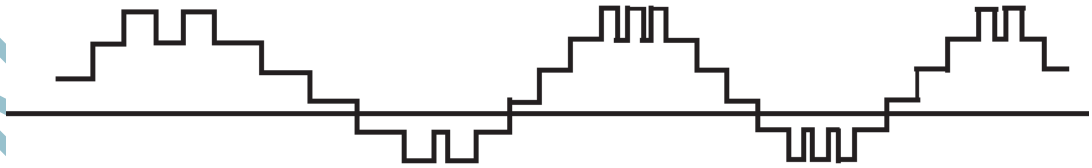


Modulating Signal I/P

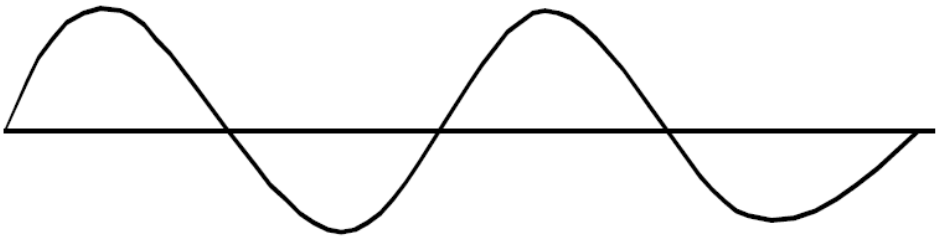
Clock I/P



Delta Modulator O/P



D/A Output



Filtered Output

7. FREQUENCY SHIFT KEYING

Aim: To study frequency shift key (FSK) Modulator and Demodulator

Apparatus :

1 . FSK Modulator-FSK Demodulator.

2 . Function Generator.

3. CRO.

4 . BNC Probes.

Theory:

In this method, the binary signal u (t) is used to generate a waveform.

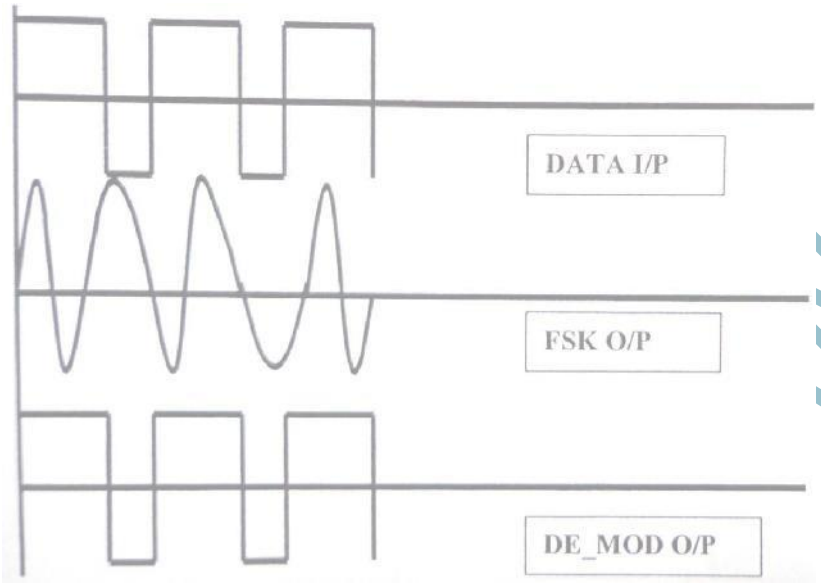
$$V_{FSK}(t) = A \cos (Wo \pm U) t$$

The pulse sign is applied when v (t) = +V and minus sign is applied when V (t) =- V. Thus the frequency of transmitted signal is high for 1 and low for a 0. A straight forward way to detect an FSK signal is to use a suitable filter of sharp cut-off.

PROCEDURE :

1. Connect the output of the carrier o/p provided on kit to the input of carrier i/p1 terminal.
2. .Also connect one of the data output to the data input terminal provided on kit.
3. Connect sinwave of certain frequency to the carrier i/p2 terminal.
4. Switch ON function generator and FSK modulation and demodulation Kit.
5. Observe the FSK o/p by connecting it to CRO. Thus FSK modulation can be achieved.
6. For FSK demodulation, connect FSK o/p terminal to the FSK i/p terminal of demodulator.
7. Observe the demodulated wave at demodulated o/p terminal by connecting it to CRO.

Model Waveforms:



Observations:

Data input:

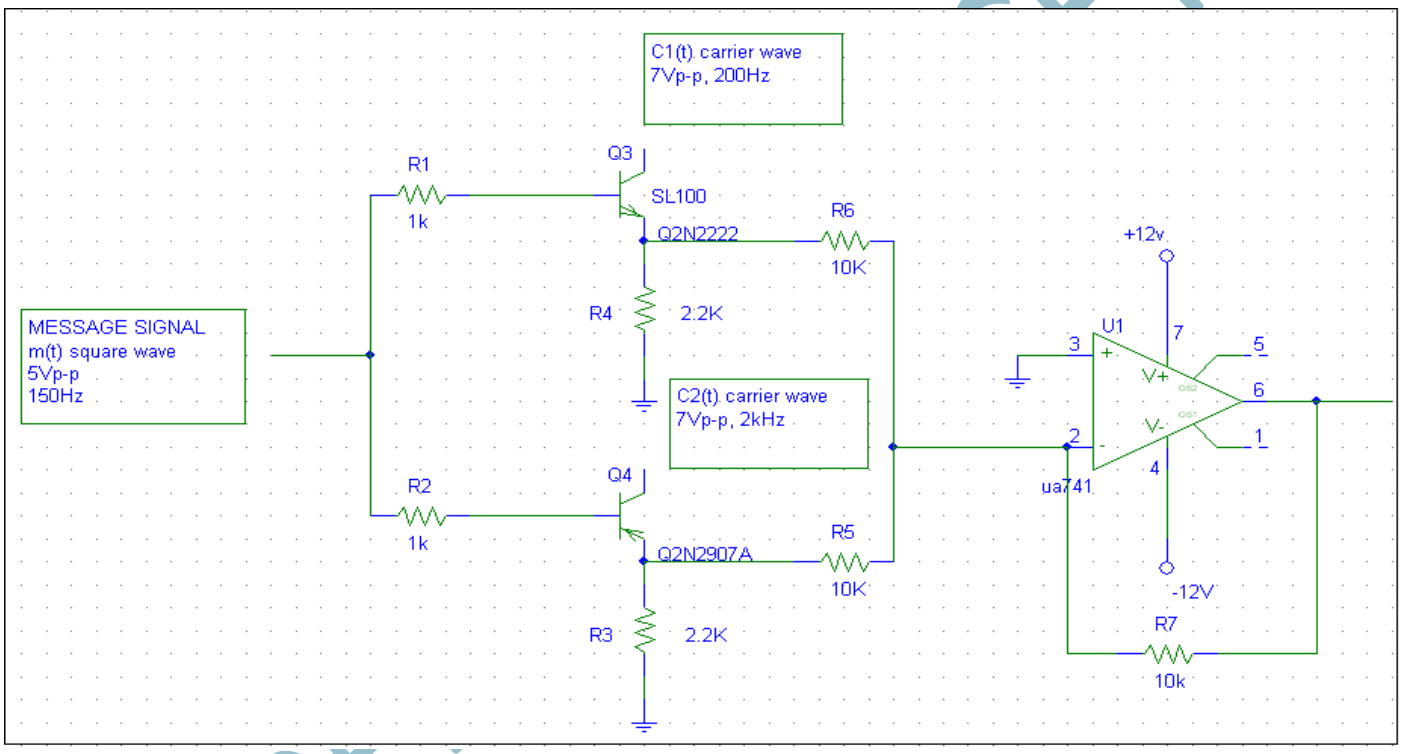
Waves	Amplitude V(volts)	Duration of Bits (micro seconds)	
		Bit 1	Bit0
Data input-1			
Data input-2			
Data input-3			
Data input-4			

Carrier input:

Waves	Amplitude(V_{p-p}) (volts)	Frequency(KHz)
Carrier input-1		
Carrier input-2		

PROCEDURE:

MODULATION CIRCUIT:



DESIGN

Let I_C =1mA, β = 30, V_{CE}sat = 0.2V, V_{BE} = 0.7V
Applying KVL to collector loop:
V_{CE}sat + V_{RE}+ I_ER_E = 7/2 => 0.2V+ 0.7V+IERE = 3.5V
i.e., I_ER_E = 3.5 – 0.2 – 0.7
RE = 3.3kΩ
Therefore, RE = 3.3kΩ

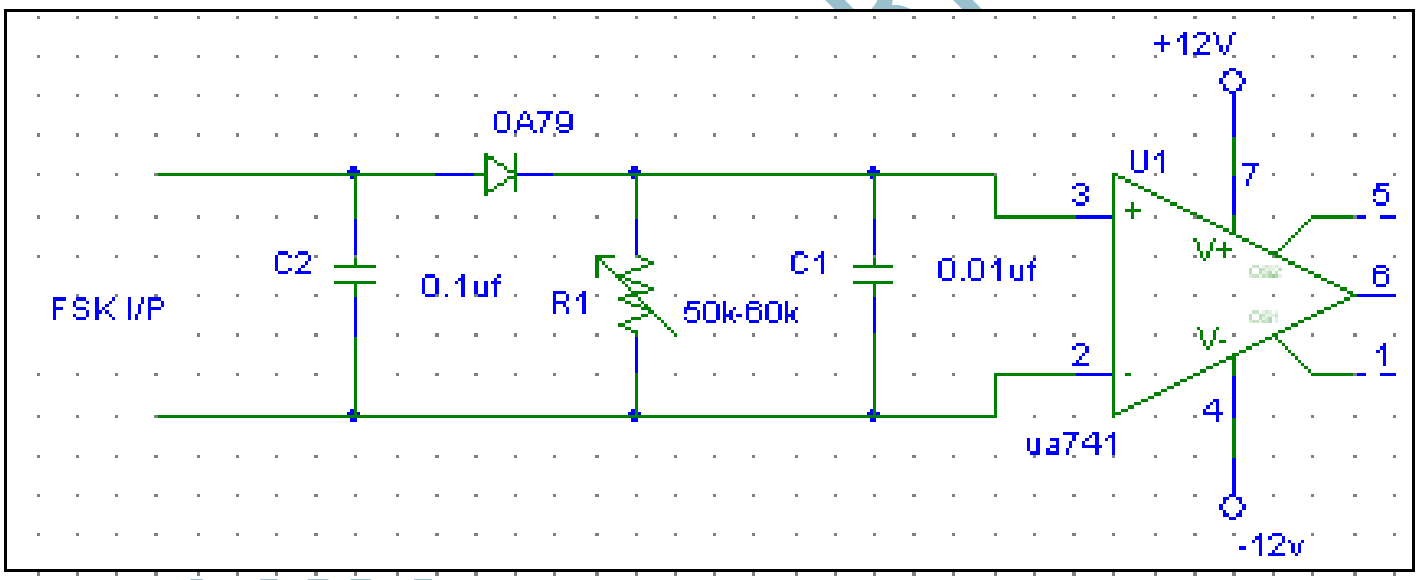
KVL to the emitter loop results in the equation
I_BR_B + V_{BE} + V_{RE} = 5/2
Therefore, RB = 22kΩ
$2\pi R_1C_1$ = 1m,
If C_1 = 0.1μf
R_1 = 1.59kΩ

PROCEDURE:

PROCEDURE:

1) The connections are made as per the circuit diagram.
2) Message signal of amplitude 5v and frequency 150 Hz is applied to the base of the transistor
3) Carrier $C_1(t)$ of 200Hz and 7v is applied at the collector of the NPN transistor.
4) Another carrier $C_2(t)$ of 2 kHz and 7v is applied at the Collector of the PNP transistor.
5) After getting the FSK output waveform, calculate
   i. t_{max} and t_{min} . Therefore $f_{max} = 1 / t_{max}$ and
   ii. $f_{min} = 1 / t_{min}$.
6) Calculate the frequency deviation as $\Delta f = f_{max} - f_{min}$
7) Calculate the modulation index, $\beta = \Delta f / f_m$.
8) Then apply the FSK output to the input of the Demodulation circuits and gets the demodulated output.

DE- MODULATION CIRCUIT:



PROCEDURE:

1) Connections are made as shown in the demodulation circuit diagram above.
2) The FSK output is fed as the input to the demodulator circuit.
3) The DRB/POT are slowly tuned to obtain the desired demodulated waveform which is the square wave message signal.

Note:-

1) Please not that the tuning of the potentiometer/DRB has to be gradual.
2) The signal generators of carriers also can be varied gradually within the limits of the design for amplitude or frequency.

Result: Design and study the working of FSK modulation and demodulation is done successfully

8. PSK MODULATION& DEMODULATION

AIM:

To study the various steps involved in generating the phase shift keyed signal at the modulator end and recovering the binary signal from the received PSK signal.

Apparatus:

1. PSK Modulation & Demodulation
2. CRO
3. Connecting Wires

Theory:

Phase shift keying is one of the most efficient digital modulation techniques. It is used for very high bit rates. In PSK, the phase of the carrier is modulated to represent Binary values. In BPSK, the carrier phase is used to switch The phase between 00 and 1800 by digital polar Format. Hence it is also known as phase reversal keying. The modulated carrier is given by:

$$\text{Binary 1: } S(t) = Ac_{max}. \cos(2\pi fct)$$

$$\text{Binary 0: } S(t) = Ac_{max}. \cos(2\pi fct + 180)$$

$$= - Ac_{max}. \cos(2\pi fct)$$

If the carrier phase is shifted between two values then the method is called Phase Shift keying (PSK). In PSK the amplitude of the carrier remains constant.

To generate a binary PSK signal, we have to represent the input binary sequence in polar form with symbols 1 and 0 represented by constant amplitude levels of $+\sqrt{E}_b$ and $-\sqrt{E}_b$, respectively. This signal transmission encoding is performed by a polar non return – to – zero (NRZ) level encoder. The resulting binary wave and a sinusoidal carrier $\varphi(t)$, whose frequency $f_c = (n_c / T_b)$ for some fixed integer n_c, are applied to a product modulator as shown fig.1. The carrier and the pulses used to generate the binary wave are usually extracted from a common master clock. The desired PSK wave is obtained at the modulator output. To detect the original binary sequence of 1s and 0s, we apply the noisy PSK signal $x(t)$ (at the channel output) to a correlator, which is also supplied with a locally generated coherent reference signal $\varphi_1(t)$ as shown fig.2. The correlator output, X_1 is compared with a threshold of zero volts. If $X_1 < 0$, it decides in

favour of symbol 0.
If X1 is exactly zero, the receiver makes a random guess in favour of 0 or 1.

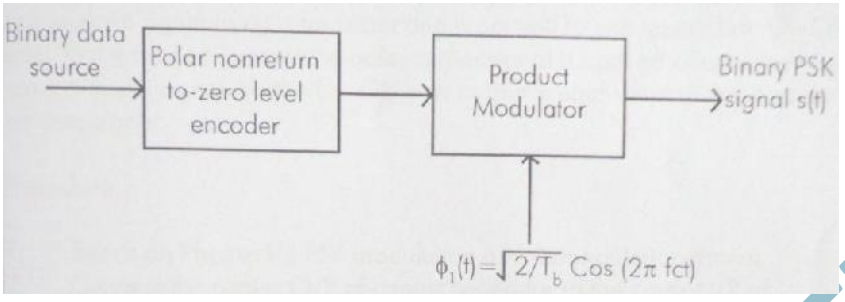
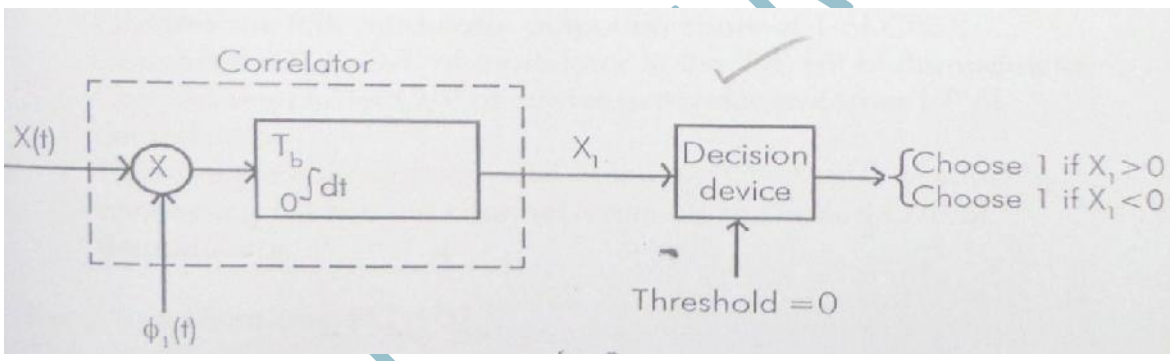


Fig1.Block diagram for BPSK transmitter

Fig2. Block diagram of BPSK receiver



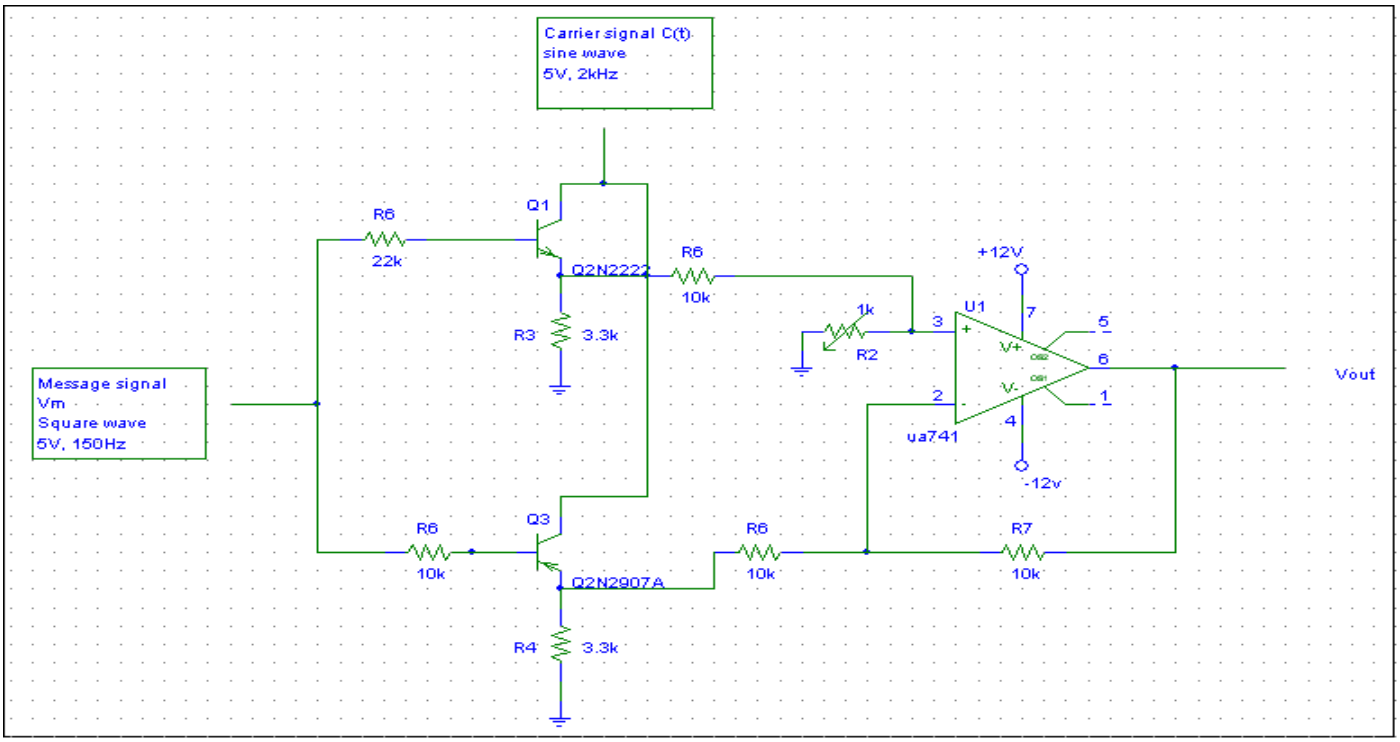
In PSK modulation and demodulation, the IC 8038 is a basic wave form generator which generates sine, Triangle and square waveforms. The sine wave generated by this 8038 IC is used as carrier signal to the system. The square wave generated by IC 8038 is at ± 12 volts level. So this is converted into a ± 5 volts signal with the help of a transistor and diode. This square wave is used as a clock input to a decade counter (IC 7490) which generates the modulating data outputs. IC CD4051 is an analog multiplex inputs of the IC. Modulating data input is applied to its control input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered to the output. The 1800 phase shift of the carrier signal is created by an operational amplifier using 324 IC.

During the demodulation, the PSK signal is converted into a +5 volts square wave signal using a transistor and is applied to one input of an EX – OR gate. To the second input of the gate, carrier signal is applied after conversion into a +5 volts signal. So the EX – OR gate output is equivalent to the modulating data signal.

Procedure:

1. Switch on PSK modulation and demodulation trainer.
2. Connect the carrier O/P of carrier generator to the carrier I/P of modulator.
3. Connect the data O/P of Data generator to the Data I/P of Modulator.
4. Connect CH1 OF CRO to Data generator o/p and CH2 to the PSK O/P of modulator.
5. Compare these two signals.
6. Connect the PSK O/P of modulator to the PSK I/P of demodulator.
7. Connect the carrier O/P of carrier generator to carrier I/P of demodulator.
8. Connect CH1 OF CRO to Data generator o/p and CH2 to the demodulator o/p.
9. Compare these two signals.

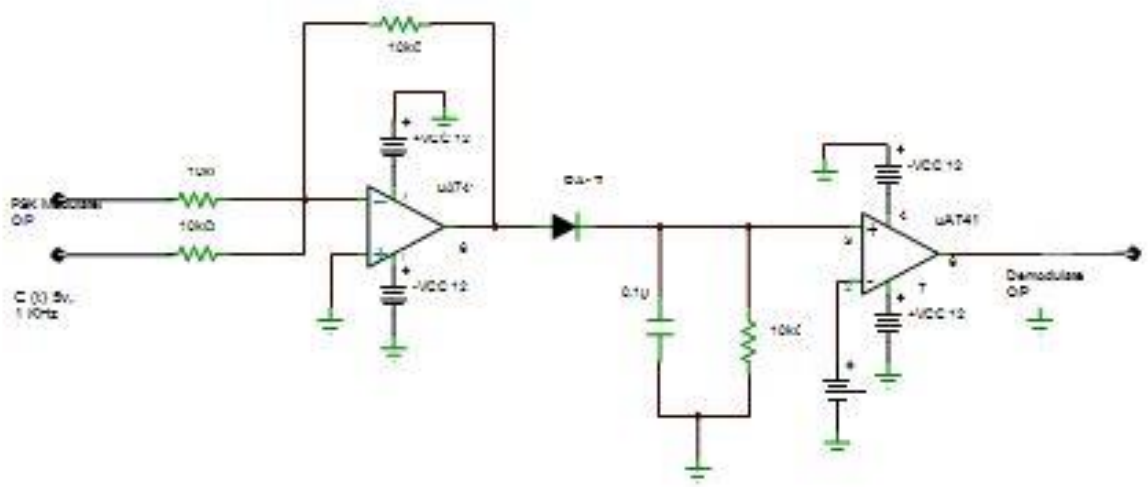
MODULATION CIRCUIT



PROCEDURE:

1) The connections are made as per the circuit diagram.
2) A sine wave of amplitude 5v and 2kHz is fed to the Collector of the transistor as carrier.
3) the message signal, a square wave of amplitude 5V and 150Hz is fed to the base of the transistor.
4) The BPSK wave is observed at pin 6 of the op-amp IC 741.
5) The demodulation circuit is also connected.
6) BPSK wave obtained is fed as input to the demodulation circuit.
7) The demodulated waveform is observed
8) All the required waveform to be plotted.

DEMODULATION CIRCUIT



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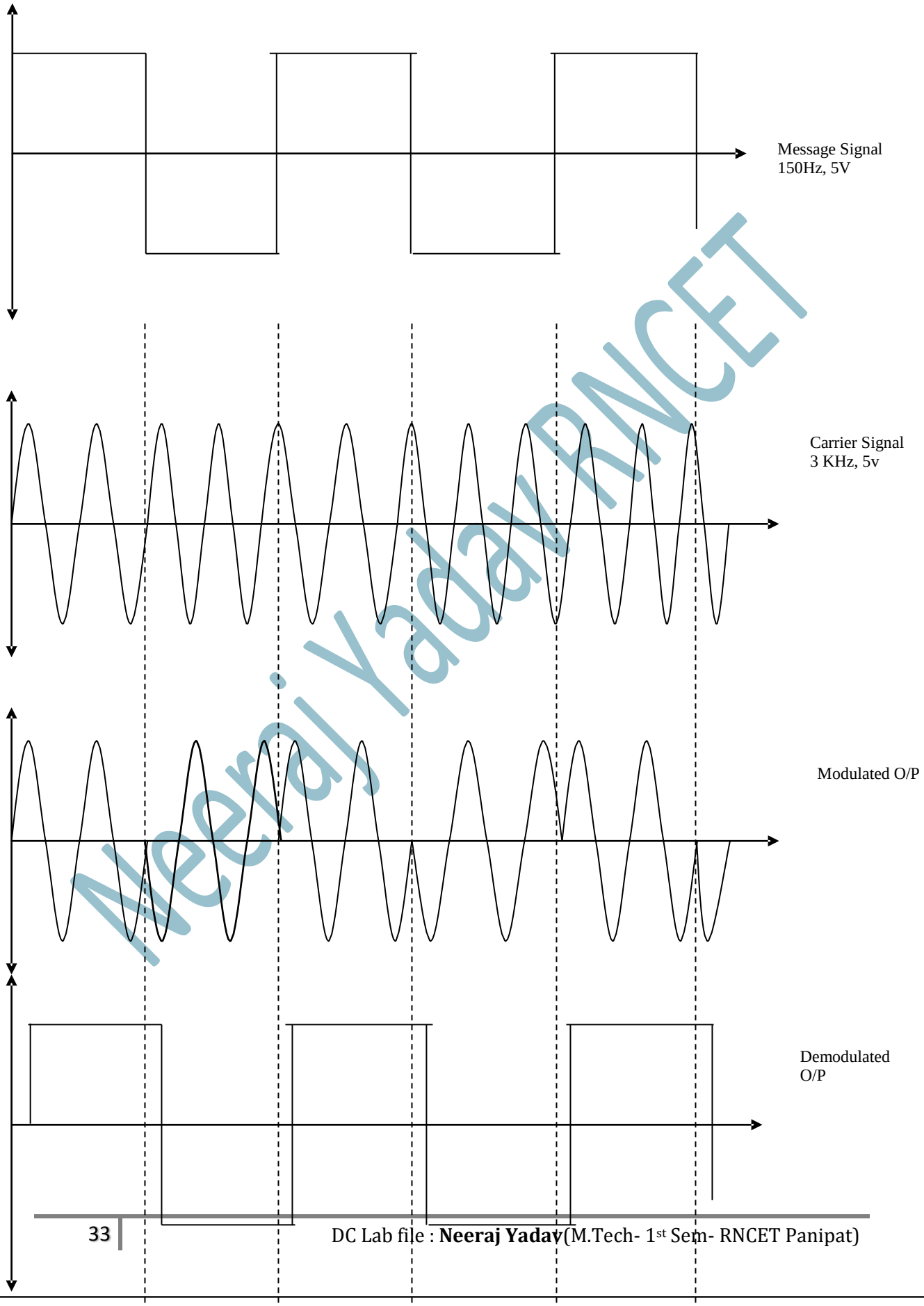
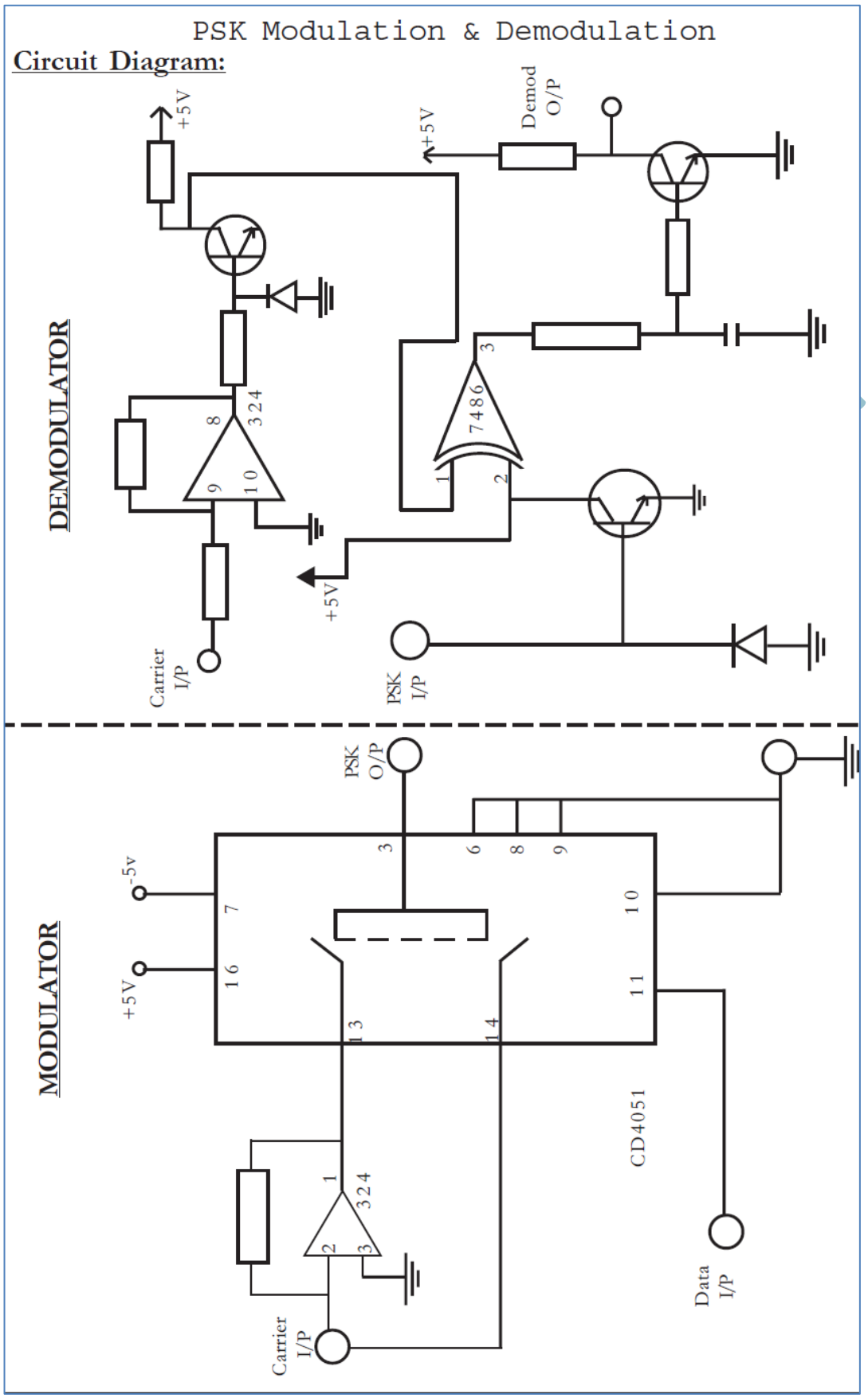


PSK Modulation & Demodulation

Circuit Diagram:



9. DIFFERENTIAL PHASE SHIFT KEYING

Aim: To study the various steps involved in generating differential phase shift keyed signal at the modulator end and recovering the binary signal from the received DPSK signal.

APPARATUS :

1. Differential Phase shift keying Trainer.
2. CRO
3. Connecting Wires.

Theory:

DPSK may be viewed as the non-coherent version of PSK. It eliminates the need for a coherent reference signal at the receiver by combining two basic operations at the transmitter:

1. Differential encoding of the input binary wave and
2. Phase-Shift Keying hence, the name, differential phase shift keying (DPSK).

In effect to send symbol 0, we phase advance the current signal wave-form by 1800, and to send symbol 1, we leave the phase of the current signal waveform unchanged. The receiver is equipped with a storage capability, so that it can measure the relative phase difference between the waveforms received during two successive bit intervals. Provided that the unknown phase θ contained in the received wave varies slowly, the phase difference between wave forms received in two successive bit intervals will be independent of θ.

The block diagram of a DPSK transmitter is shown in fig.1 below. It consists, in part of a logic network and a one-bit delay element interconnected so as to convert the binary sequence {b k} into a differentially encoded sequence {d k}. This sequence is amplitude level encoded and then used to modulate a carrier wave of frequency fc, thereby producing the desired DPSK signal.

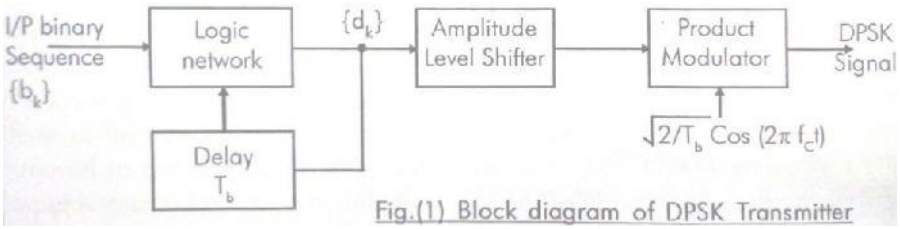


Fig.(1) Block diagram of DPSK Transmitter

The optimum receiver for differentially coherent detection of binary DPSK is as shown in fig.2 below. This implementation merely requires that sample values be stored, thereby avoiding the need for delay lines that may be needed otherwise. The equivalent receiver implementation that tests squared elements is more complicated, but its use makes the analysis easier to handle in that the two signals to be considered are orthogonal.

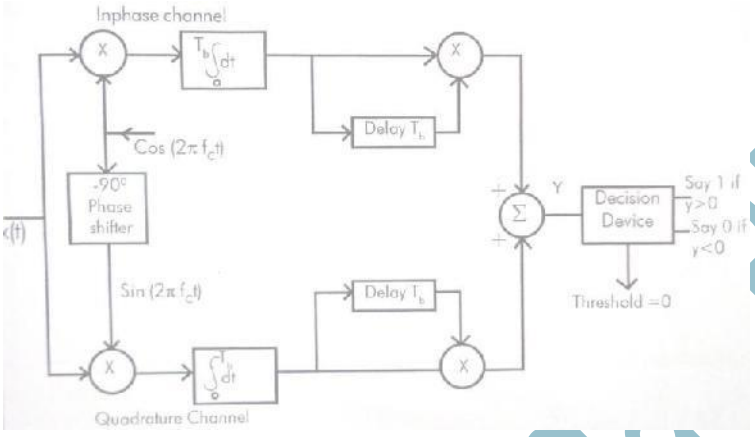


Fig2. Block diagram of DPSK receiver

In DPSK modulation and demodulation, the IC8038 is a basic waveform generator which generates sine, square, triangle waveforms. The sine wave generated by this 8038 IC is used as carrier signal to the system. The square wave generated by 8038
IC is at +/_ 12v level. So this is converted into a +5v signal with the help of a transistor and diode. This square wave is used as a clock input to a decade counter(IC 7490) which generates the modulating data outputs.

The differential signal to the modulating signal is generated using an exclusive-OR gate and a 1-bit delay circuit.CD 4051 is an analog multiplexer to which carrier is applied with and without 180 degrees phase shift(created by using an operational amplifier connected in inverting amplifier mode) to the two inputs of the IC741. Differential signal generated by EX-OR gate (IC 7486) is given to the multiplexers control signal input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered to the output. One-bit delay generation of differential signal to the input is created by using a D-flip-flop (IC 7474).

During the demodulation, the DPSK signal is converted into a +5v square wave signal using a transistor and is applied to one input of an EX-OR gate. To the second input of the gate, carrier signal is applied after conversion into a +5v signal. So the, EX- OR gate output is equivalent to the differential signal of the

modulating data. This differential data is applied to the one input of an Exclusive-OR gate and to the second

input, after one-bit delay the same signal is given. So the output of this EX-OR gate is modulating signal.

PROCEDURE :

1. Switch on differential Phase shift Keying trainer.
2. Connect the carrier output of carrier generator to the 13th pin of CD4051 (Analog mux) of modulator.
3. Connect the Bit clock output to the Bit clock input at pin 3 of 7474 (8-bit converter) of modulator.
4. Connect the data output of data generator to the input of modulator circuit.
5. Connect channel 1 of CRO to the data generator.
6. Observe the differential data output at pin 2 of 7474 IC on channel -1 of CRO.
7. Observe the DPSK modulated output on channel-2 of CRO.
8. During demodulation, connect the DPSK modulated output to the DPSK I/P of Demodulator.
9. Connect the Bit clock O/P to the Bit clock I/P of Demodulator and also connect the carrier O/P to the carrier I/P of demodulator.
10. Observe the demodulated data O/P at demodulator.
11. The frequency of modulation data signal should be equal to the demodulated O/P.

Observations:

Carrier voltage = 5.04volts; Carrier frequency = 5.618 K Hz.

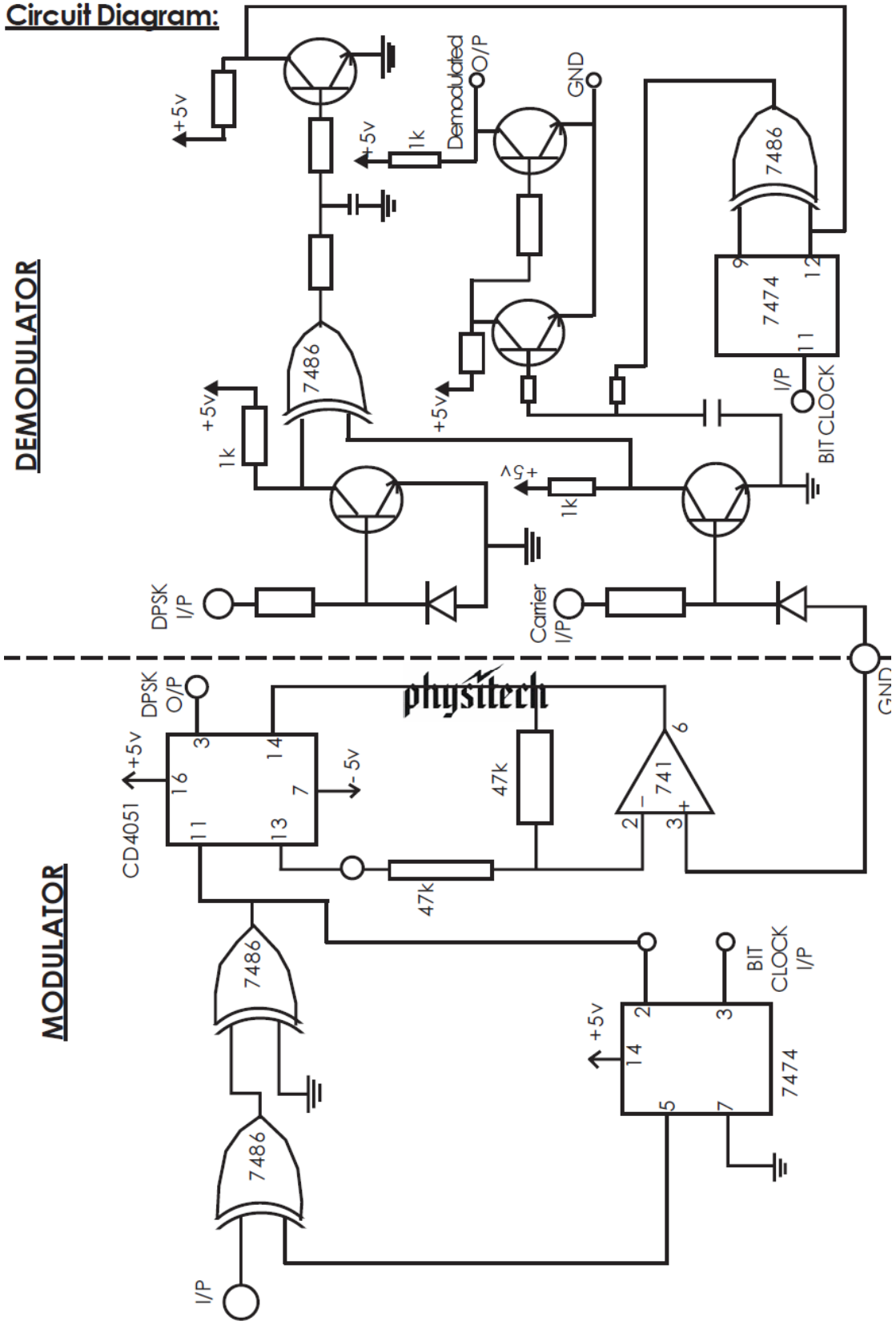
Waves	Amplitude(volts)	Duration of Bits (micro seconds)	
		Bit 1	Bit 0
Data input-1			
Data input-2			
Data input-3			
Data input-4			

Bit clock voltage = ; clock on-time =
clock off-time =

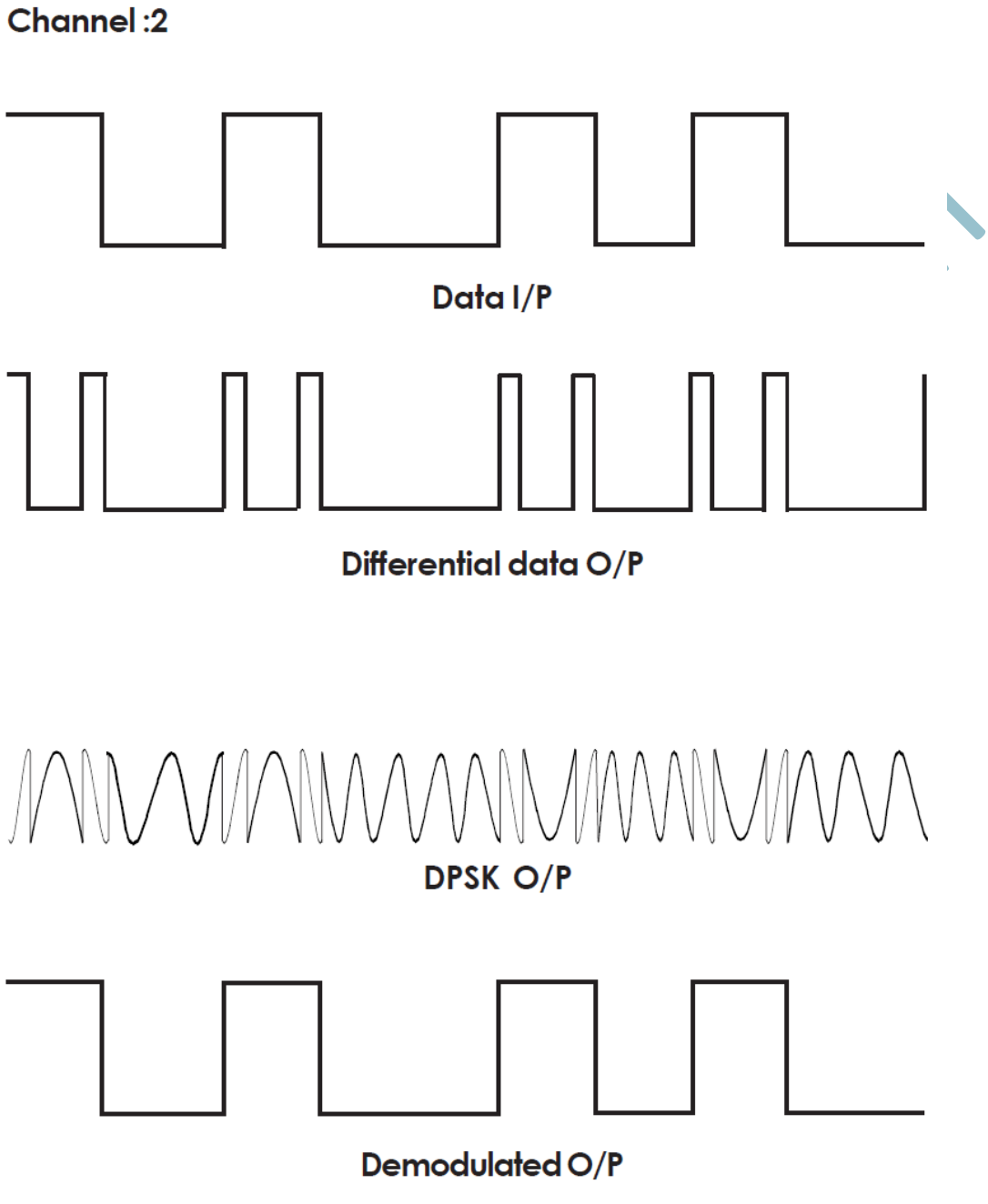
Differential output corresponding to	Amplitude(volts)	Duration of Bits (micro seconds)	
		Bit 1	Bit 0
Data input-1			
Data input-2			
Data input-3			
Data input-4			

Differential Phase Shift Keying

Circuit Diagram:



EXPECTED Waveforms



Result: DPSK is studied successfully